AN10896

Mounting and Soldering of RF transistors

Rev. 01 — 17 May 2010 **Application note**

Document information

Info	Content
Keywords	Surface mount, reflow soldering, bolt down
Abstract	This application note provides bolt down and soldering guidelines for NXP's RF transistor packages

Revision history

Rev	Date	Description
01	20100517	Initial release

Contact information

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1. Introduction

1.1 General (mounting recommendations RF power)

This document is intended to guide customers in ways how to mount and solder RF Power transistors. The typical frequency bands involved range from 800 Mhz up to 3.5 Ghz. It includes packages ranging from the Base station, Broadcast and Microwave applications. Each customer has its own way of designing applications and mounting the devices, so therefore not possible to cover all specific requirements. The intention of this document is to have a general mounting recommendation/guideline suitable for each individual device, whether it is a ceramic or a plastic over-molded package.

1.2 Definition

The following words in this document:

“Heat sink” refers to the heat sink located under the PCB, the application heat sink.

“Exposed heat spreader” is used for plastic over molded devices.

"Flange" (also a heat spreader) is used for the ceramic devices.

"Eared" is a flange with 2 slotted holes allowing bolt down.

"Earless" is a flange used for devices that are being soldered.

"Foot Print or Solder land" is used to define the area on which to solder.

1.3 Main product groups

The introduction of LDMOS transistors started with the use of an air cavity package. The construction consists of a metal flange with on top an insolated ring frame with leads. The X-tals and in- and output capacitors are eutectic soldered onto the flange. Gold wire bonds (later Aluminum) where used to make the connection between the lead and the X-tal. As a final step the package is closed with a lid, see illustration. Typically these packages where bolted down to a heat sink, while the lead are hand soldered to the PCB board.

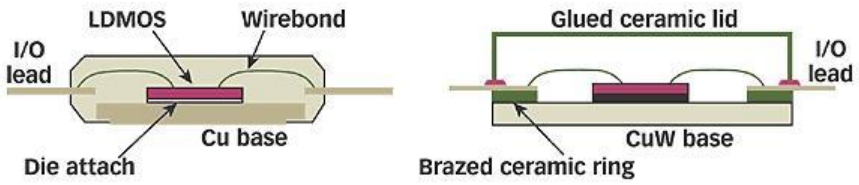


Fig 1. Over-molded versus air cavity based package

Some customer do prefer the air cavity packages to be reflow-ed in their application, meaning no thermal compound/paste under the flange but solder as well, as was already used to make the connect the lead to the PCB. Main reasons to follow this route are thermal conductivity and as a result of that better mean time between failures (MTTF). Plastic over molded packages came on the roadmap somewhat later. Price pressure and technical feasibility of packaging at such high frequency devices have been the major factors in starting to follow this additional route. With the arrival of plastic over molded packages came also the request for straight as well as gull wing (surface mount) leaded packages. This document is divided in 2 main product groups: *“Air Cavity Packages”* and *“Over Molded packages”* (OMP).

2. Design rules for PCB design

2.1 Air cavity devices

2.1.1 SMDP

If the solder mask extends onto the solder lands, the remaining solder-able area is solder mask defined or also called a SMDP (solder mask defined pad). The “effective” solder pad is equal to the copper area that is not covered by solder mask. This situation is illustrated in Fig 2.

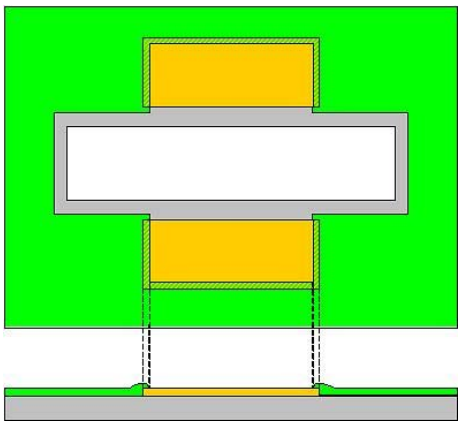


Fig 2. Solder Mask Defined Pads (SMDP)

In case of a SMDP, the copper will normally extend 75 μm underneath the solder mask on all sides; in other words, the copper dimension is 0.15 mm larger than the solder mask dimension. These values may vary depending on the class of PCBs used. This allows for tolerances in copper etching and solder mask placement, during PCB production. In Fig 2, the copper underneath the solder mask is shown in an orange/green hatch. It is possible to design a solder mask bridge in between the pads and the PCB aperture. This is illustrated in Fig 3.

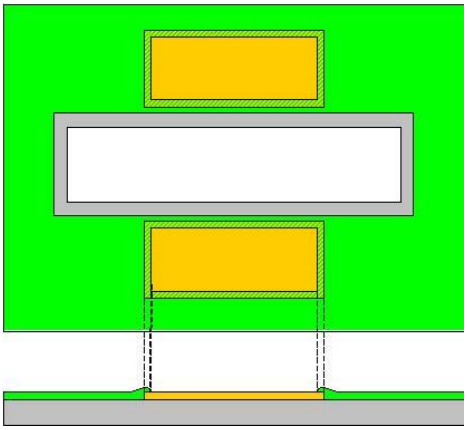


Fig 3. SMDP with solder mask bridge

If a solder mask bridge is designed between the pads and the PCB aperture, the leads will lay over this bridge. For SMDPs, the lead will hover (see Fig 4.) a little above the copper. This should not present a problem, as the ridge will only be, at most, 10 μm high, but it does mean that the gap has to be filled with solder during the soldering process.

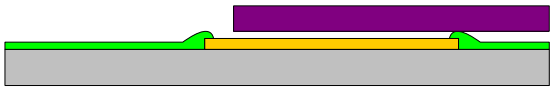


Fig 4. Lead resting on a SMDP

2.1.1.1 Foot print dimensions SMDP

When it comes to defining the dimensions of the footprint on the PCB, only a few of the package dimensions are relevant. These are summarized in Fig 5.

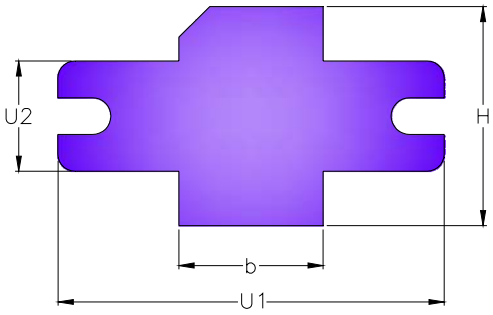


Fig 5. Relevant package dimensions for footprint definition

2.1.1.2 PCB Aperture dimensions

The package body is placed through an aperture in the PCB, and onto the heat sink. The dimensions of the aperture in the PCB should be such that the package can be comfortably inserted through it. In general, apertures in a PCB are made with certain accuracy.

Therefore it is advisable to design the PCB aperture larger than the maximum package body dimensions in that way there will always be at least 200 μm left for package insertion.

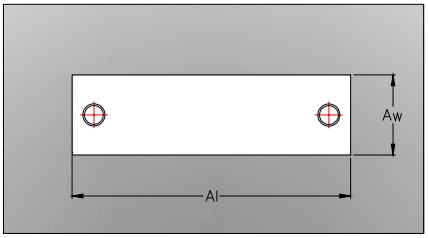


Fig 6. PCB aperture dimensions

Aperture dimension (Al and Aw) =

U_{max} + 0.2 (allow insertion) + aperture accuracy fabrication (typically 0.2)

Because of the production method, the radius at the corner of an aperture is at least 0.4 mm. For easy insertion of the package through the PCB, it is advised that the minimum radius is used in PCB design. The copper and solder mask dimensions for the air cavity packages are summarized in Fig 7. and Fig 8. This is for the SMDP situation.

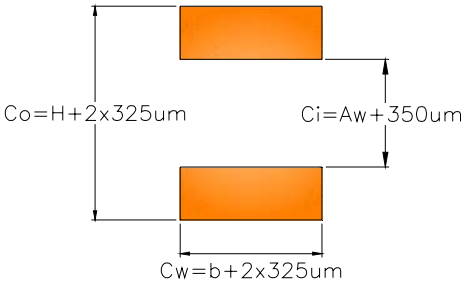


Fig 7. Cu footprint dimensions for SMDP

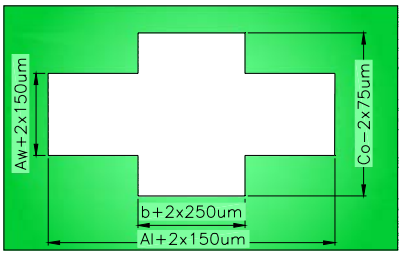
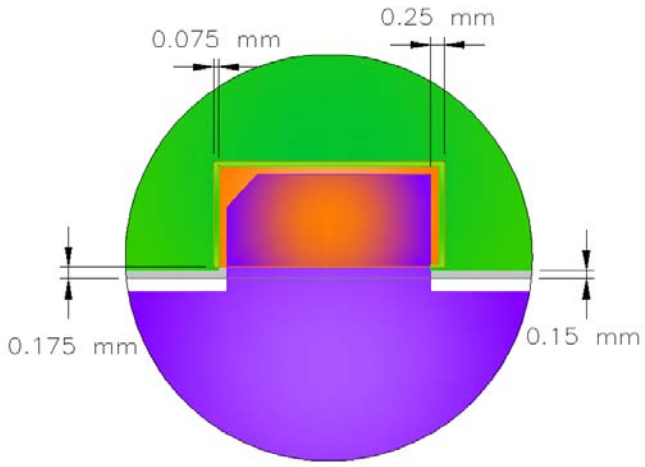


Fig 8. Solder land/resist/mask dimensions for SMDP

The main rules used to define the footprint dimensions are:

- The solder mask apertures are 250 μm larger than the package leads, on the three outer sides (the total dimensions are 500 μm larger). This value is relatively large, so that placement accuracy of the package on the PCB is not critical.
- The copper extends 75 μm underneath the solder mask on all sides, i.e. the total dimensions are 150 μm larger than the copper dimensions.
- The solder mask must lay 150 μm away from the aperture on all sides.
  If a solder mask ridge is designed between the PCB aperture and the pads, it must be at least 100 μm wide.

The main rules are summarized in Fig 9.



Purple = package/lead edge

Grey = edge of PCB aperture

Orange = edge of Cu

Green = edge of solder mask aperture

Fig 9. Main rules in defining the SMDP foot print

2.1.2 NSMDP

If the solder mask layer starts outside of the solder lands, and does not cover the copper, this is referred to as Non Solder Mask Defined Pad (NSMDP). The “effective” solder pad is equal to the copper area.

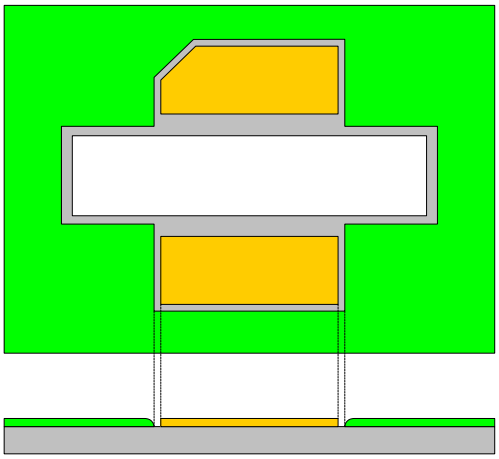


Fig 10. Non Solder Mask Defined Pads (NSMDP)

In case of a NSMDP, the solder mask must be at least 75 μm away from the solder land on all sides. In other words, the solder mask dimension is 150 μm larger than the copper dimension. These values may vary depending on the class of PCBs used. The main requirement is that the solder mask is far enough away from the copper, so that – with the given tolerances in solder mask application – it does not extend onto the copper. This is shown in Fig 10. In the figure, color Grey is bare FR4, orange is copper, and green is solder mask. Basically, there is a large trench in the solder mask, around the copper.

The ceramic package is placed through an aperture in the PCB. This aperture is indicated by the white rectangle. Note that the solder mask does not reach the edge of the PCB aperture: it must always be at least 150 μm away from the edge of the aperture.

If so desired, it is also possible to design a narrow bridge of solder mask between the pads and the aperture in the PCB. This is illustrated in Fig 11. This is not strictly necessary, as the PCB material is also non-solder-able. Note that a solder mask bridge must have a minimum width of 100 μm.

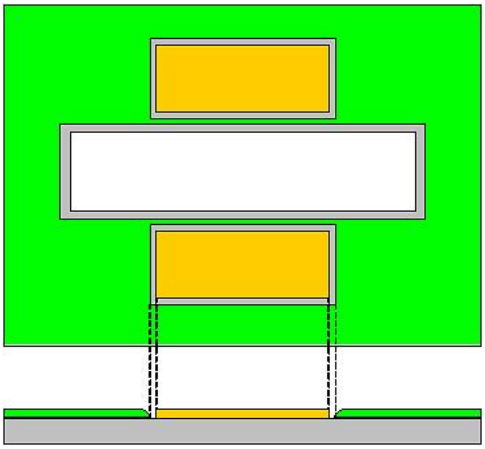


Fig 11. NSMDP with solder mask bridge

For NSMDPs, this situation is shown in Fig 12. Usually a solder mask layer is roughly 20 μm thick, whereas the copper is 30 μm – 35 μm thick. Thus, the solder mask will be lower than the copper, and the lead will rest on the copper.

Fig 12. Lead resting on a NSMDP

2.1.2.1 PCB footprint – Dimensions NSMDP

When it comes to defining the dimensions of the footprint on the PCB, only a few of the package dimensions are relevant. These are summarized in Fig 13.

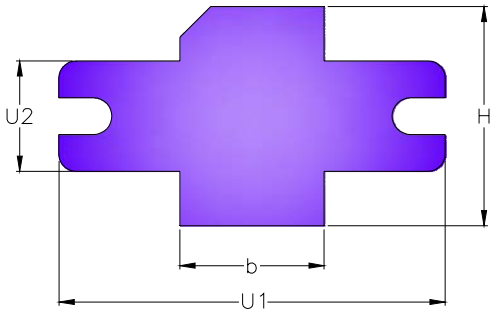


Fig 13. Relevant package dimensions for footprint definition

2.1.2.2 PCB aperture Dimensions

The package body is placed through an aperture in the PCB, and onto the heat sink. The dimensions of the aperture in the PCB should be such that the package can be comfortably inserted through it. In general, apertures in a PCB are made with certain accuracy.
Therefore it is advisable to design the PCB aperture larger than the maximum package body dimensions in that way there will always be at least 200 μm left for package insertion.

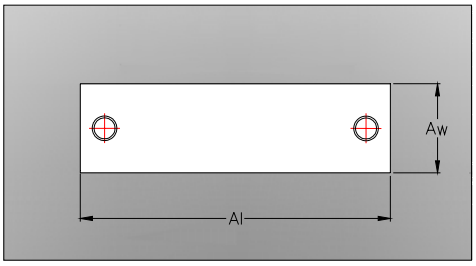


Fig 14. PCB aperture dimension

Aperture dimension (Al and Aw) =

U_{max} + 0.2 mm (allow insertion) + aperture accuracy fabrication (typically 0.2 mm)

Because of the production method, the radius at the corner of an aperture is at least 0.4 mm. For easy insertion of the package through the PCB, it is advised that the minimum radius is used in PCB design.

The copper and solder mask dimensions for the air cavity packages are summarized in Fig 15 and Fig 16. This is for the NSMD situation. Note: the 45 degrees drain lead angle (used for some outlines) is considered as being negligible and therefore not taken into account in the solder mask / foot print designs.

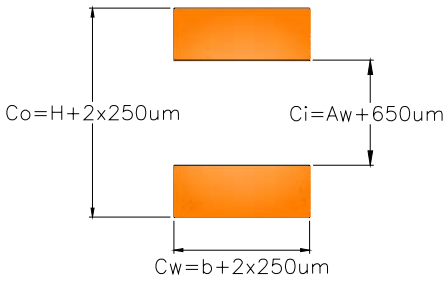


Fig 15. Cu foot print dimensions for NSMDP

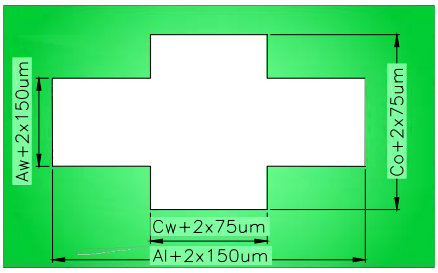


Fig 16. Solder mask/resist/land dimensions for NSMDP

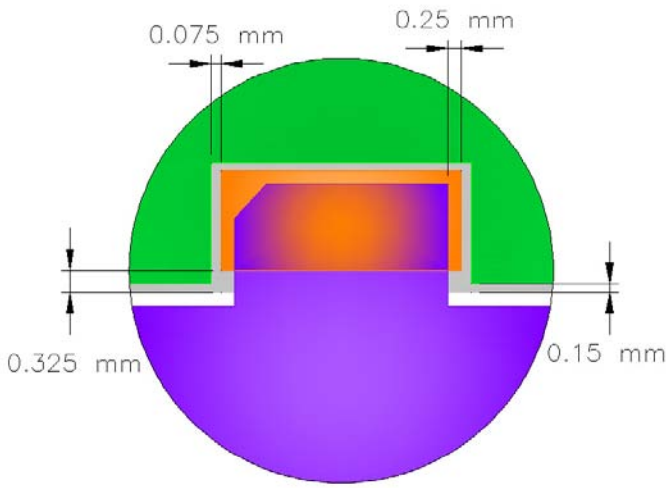
The main rules used to define the copper footprint dimensions are:

- The copper pads are 250 μm larger than the package leads, on the three outer sides (the total dimensions are 500 μm larger). This value is relatively large, so that placement accuracy of the package on the PCB is not critical.
- The distance between the two copper pads is equal to the aperture dimension, plus 325 μm per side, to accommodate 100 μm of solder mask if desired. In other words, the copper lies 325 μm away from the aperture.

The main rules used to define the solder mask dimensions are:

- The solder mask must lay 150 μm away from the aperture
- Must be at least 100 μm wide
- And it must also lay 75 μm away from the copper. The solder mask lays 75 μm outside the copper on all sides, i.e. the total dimensions are 150 μm larger than the copper dimensions.

The main rules are summarized in Fig 17.



Purple = package/lead edge

Grey = edge of PCB aperture

Orange = edge of Cu

Green = edge of solder mask aperture

Fig 17. Main rules in defining the NSMDP

2.2 Over molded devices

A footprint design describes the recommended dimensions of the solder lands on the PCB, to make reliable solder joints between the semiconductor package and the PCB.

For semiconductor packages with a small pitch it is not possible to apply a solder resist bridge between two terminals, and a Cu defined or combination layout must be used.

If a solder land is solder resist defined, the Cu must extend far enough underneath the solder resist to allow for tolerances in Cu etching and solder resist placement during board production. Similarly, if a solder land is Cu defined, the solder resist must lie sufficiently far away from the solder land to prevent bleeding of the solder resist onto the Cu pad. Typical values for these distances are 50 μm to 75 μm. The footprints referred to in this document indicate the areas that can be soldered.

2.2.1 SMD

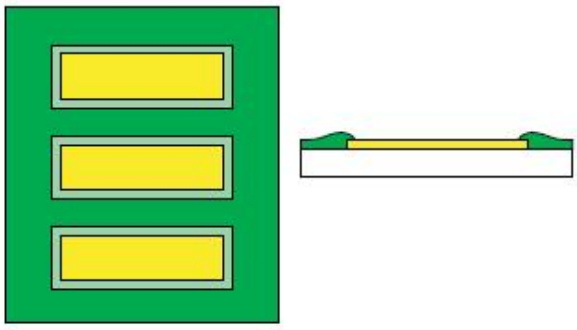


Fig 18. Solder mask/resist defined footprint (SMDP)

Figure 18 shows the solder resist defined pads; yellow is Cu and dark green is solder resist. The Cu underneath the solder resist is shown in a lighter shade of green. The alternative situation is that the solder resist layer starts outside of the Cu. In that case, the solder lands are Cu defined. This is sometimes referred to as a Non Solder Mask Defined Pad (NSMDP).

2.2.2 NSMDP

A Cu defined layout is shown in Fig 19. (White is the bare board).

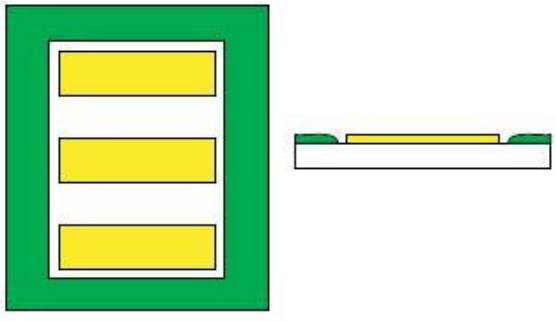


Fig 19. Cu defined footprint (NSMDP)

Note that a solder resist defined layout requires the application of a solder resist bridge between two terminals. There is a minimum width of solder resist that can be applied by

board suppliers. This fact, in combination with a maximum solder resist placement accuracy, implies that solder resist defined layouts are not always possible.

A foot print design describes the recommended dimensions of the solder lands on the PCB, to make reliable solder joints between the semiconductor package and the PCB.

The package outline and PCB footprints of NXP semiconductor plastic packages can be found by clicking “Packages” in the “Looking for products” panel on the product information page of the NXP Semiconductors web site at the URL given in “Contact information” at the bottom of page 2. The unique identifier for the PCB footprint is the NXP package outline code (the package SOT or SOD number).

For general guidelines on board design, see IPC-7351 (paragraph 12): Generic requirements for surface mount devices and land pattern standard.

The next paragraph explains how to read the PCB footprint. Fig 20 shows an example of a PCB footprint, as can be found on the NXP Semiconductors web site.

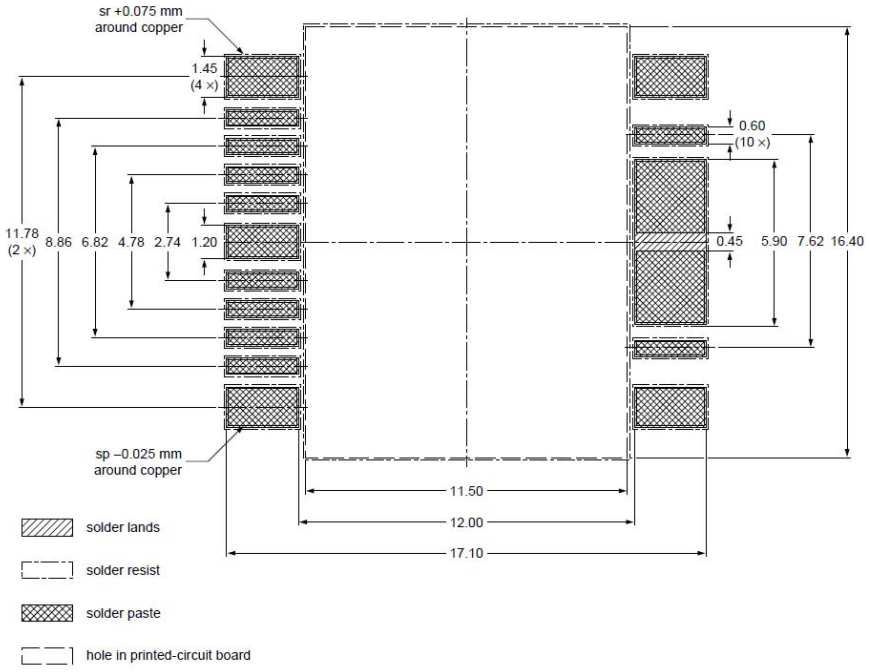


Fig 20. Example of a foot print

The soldering process is carried out under a set of process parameters that includes accuracies in the process, and semiconductor package, board, and stencil tolerances.

The footprint design is directly related to these aspects of the soldering process; the calculation of these dimensions is based on process parameters that are compliant with modern machines and a state-of-the-art process.

The substrates used for mounting the packages can be made of a variety of materials with different properties. Due to the increased transistor density in the latest semiconductor technologies, and higher current (power) handling requirements, generation of heat has become a major limitation of the semiconductor performance. By applying an exposed pad or heat sink in the semiconductor package, in combination with thermal vias in the PCB, the heat can be transferred from the active die to the outside

world. Four examples of vias capped in different ways, are shown in Fig 21. Note that the only difference lies in the solder resist pattern.

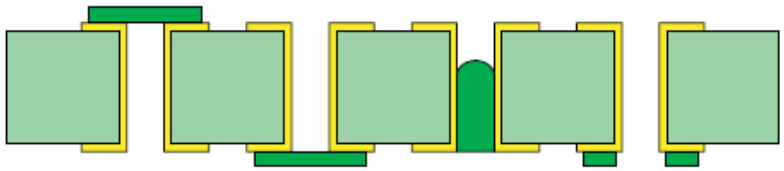


Fig 21. Capped vias; left to right: via tenting from top, via tenting from bottom, via capping from bottom, via encroached from bottom

3. Design Rules for PCB design

The heat sink design depends primarily on dissipated heat and on the other components located on the PCB. These vary from one application to the next. Therefore no general recommendations on the size and thickness of the heat sink.

The size of the cavity in the heat sink is defined by the package. For easy placement of the package flange into the heat sink cavity, the cavity width and length must be a little larger than the flange width and length. NXP recommends making both the width and the length of the heat sink cavity 100 μm larger than the flange dimensions. The formula used is similar to the one used for determining the aperture in the PCB:

Cavity dimension = U_{max} + 0.1 mm + tolerance

For the PCB, the aperture should be a little larger (+ 0.2 mm) than the cavity in the heat sink (+ 0.1 mm). This is because of the risk of positional inaccuracy of the aperture in the PCB and the ensuing risk of placing the package leads on the ridge of solder mask. This risk does not exist with the heat sink cavity. As the tolerance in the heat sink cavity varies per application, the end values are not given in this document.

For these packages, it is essential that, after mounting, the package leads make good contact with the PCB pads, and that at the same time the bottom of the flange makes good contact with the heat sink. The main parameters here are:

- The PCB thickness (Pt, see Fig 22.).
- The thickness of the interface (adhesive) between the PCB and the heat sink.
- Solder thickness under the lead.
- The height of the heat sink cavity (or pedestal) (Cd).
- The thickness of the thermal compound between the flange and the heat sink (Sf)
- Q: this is the dimension (also known as stand off/seating plane) between the bottom of the flange and the bottom of the leads. This is defined by the package.

All of these parameters will vary due to their tolerances. Determining, the to be made, cavity depth is a simple calculation of a worst case tolerance stack up; however it might end up in a value simple too large for normal production (the leads will likely lay too high above the PCB). A more common way is to make use of the Square Root of Sum of the Square method (2σ or 3σ respectively 97.3 % and 95.4 % of the population). Use the actual distribution of all valid parts. In case these are not available take the actual specification.

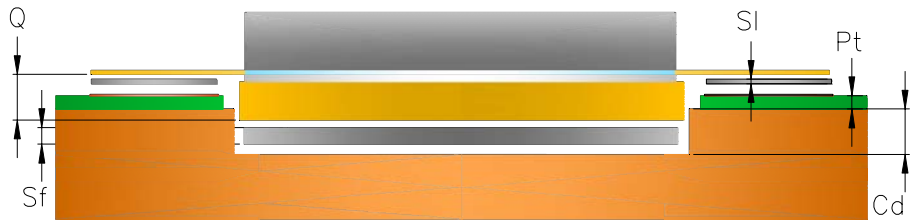


Fig 22. Main rules in defining the SMD footprint

Two main factors need to be taken into account with the design of the heat sink cavity depth:

- In a situation with a too deep cavity the leads will be lifted upwards when bolting down the flange. With a PCB edge close to the package this could lead not only to high stresses at zero hours, but during operating life (temperature differences, CTE mismatches of materials) these might even become higher. Thus it is important to test these worse case conditions prior to release the process. Another phenomena is the end of the lead tip laying high above the PCB, this might be compensated when soldering the leads.

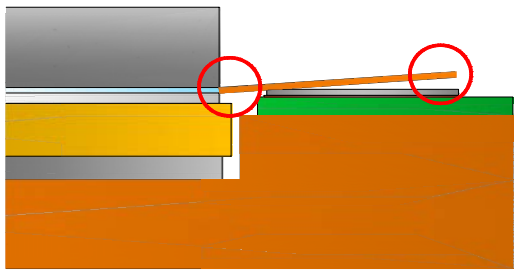


Fig 23. Main rules in defining the SMD footprint

- In a situation with a too shallow cavity the distance between the solder of the leads and the flange becomes smaller, increasing the chance of solder bridging resulting in short circuits.

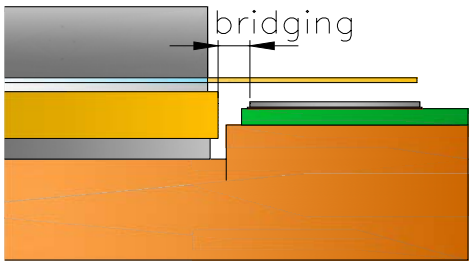


Fig 24. Main rules in defining the SMD footprint

3.1 Surface condition of the (heat sink) cavity

NXP recommends the following for bolt down applications:

- Flatness of mounting areas to be 0.01 mm.
- Roughness Ra must be less then 0.5 μm (for bolt down applications)
- Free of burrs

4. Solder paste printing

Solder paste printing requires a stencil aperture to be completely filled with paste. When the board is released from the stencil, the solder paste is supposed to adhere to the board so that all of the paste is released from the stencil aperture and a good solder paste deposit remains on the board. Ideally, the volume of solder paste on the board should equal the 'volume' of the stencil aperture. In practice, however, not all of the solder paste is released from the stencil aperture. The percentage of paste released depends largely on the aperture dimensions, that is, the length and width and the depth (the stencil thickness). If a stencil aperture becomes very small, the paste will no longer release completely. Furthermore, stencil apertures must be larger if a thicker stencil is used.

Another important factor is the aperture shape, that is, whether the aperture is rectangular, trapezoidal, or otherwise. Paste release also depends - amongst others – on the loading and speed of the squeegee, the board separation speed, the printing direction and the aperture orientation. In essence, all of these parameters must be adjusted so that all solder paste deposits on one board, from the smallest to the largest, are printed properly.

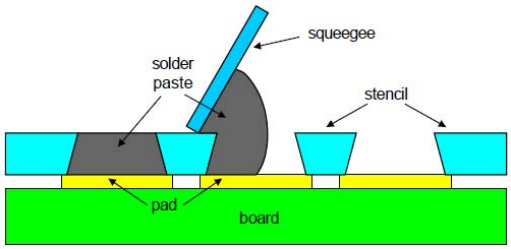


Fig 25. Stencil printing

Consequences of insufficient solder paste printing are usually open contacts or bad joints.

These may arise because:

• the solder paste deposit is not sufficiently high: components or their leads may not make proper contact with the paste, resulting in open circuits or bad joints, or

• There is insufficient solder volume for a proper solder joint, also resulting in open circuits, or

• the activator is used up rapidly in a small solder paste deposit, so that the paste no longer properly wets the component metallization, also resulting in open circuits

4.1 Stencil thickness

A second important aspect in solder paste printing is smearing. If some solder paste bleeds between the stencil and the board during one printing stroke, then the next board may not fit tightly to the stencil, allowing more paste to bleed onto the bottom of the stencil. Once this effect starts, it strengthens itself. As a result, the solder paste may eventually form bridges that stretch from one paste deposit to the next. If a bridge is narrow enough, it will snap open during reflow, as the volume of molten solder seeks to attain minimum surface area. A wider bridge, however, may remain stable, resulting in a short circuit.

To achieve a difference in solder paste volumes on one board, it is possible to use a stencil that has a different thickness at different locations. An example of this is the step-stencil. This, however, is only recommended if there is no other solution. Stencils are commonly made from Nickel; they may be either electro-formed or laser-cut (preferred). Typical stencil thickness is given in Table 1.

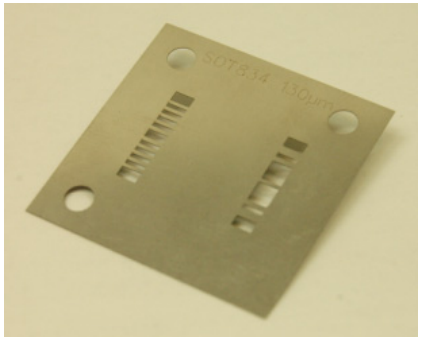


Fig 26. Stencil

Table 1. Stencil thickness

Semiconductor package pitch	Stencil thickness
≥ 0.5 mm	150 μm
0.4 mm to 0.5 mm	100 μm to 125 μm

In most cases, the package will be mounted on a PCB after the rest of the PCB has been populated. In other words, the following steps precede mounting of a package:

- Solder paste printing (sometimes in combination with a solder preform)
- Component placement
- Reflow
- Only after the above, will mounting of a package start.

II may be useful to print solder paste on the PCB pads for the air cavity package as well. This solder will have been reflow-ed by the time the package is placed. However, it will nonetheless ensure that there is some solder underneath the leads. The height of the solder on the PCB pads will depend on the stencil that was used for stencil printing.

No-clean solder paste and no-clean solder wire should be used, so the PCB and the package do not have to be cleaned after reflow- or manual soldering.

The footprint design describes the recommended solder land on the PCB to make a reliable solder joint between the semiconductor package and the PCB. A proven solder material is SnPb, but due to legislation, the industry has changed, to a large extent, to Pb-free solutions such as Sn/Ag/Cu (SAC). Process requirements for solder paste printing and reflow soldering, for SnPb and Pb-free, are also discussed in this document.

Printed-circuit boards and footprints Printed-Circuit Boards (PCBs) are not only used as mechanical carriers for electronic components; they also provide the electronic interconnection between these components and also between these components and the outside world. These electronic components may be semiconductors, or other types such as capacitors and resistors. Through component selection and the use of Cu interconnections between the components, an electronic system, such as a mobile phone, can be assembled on a PCB.

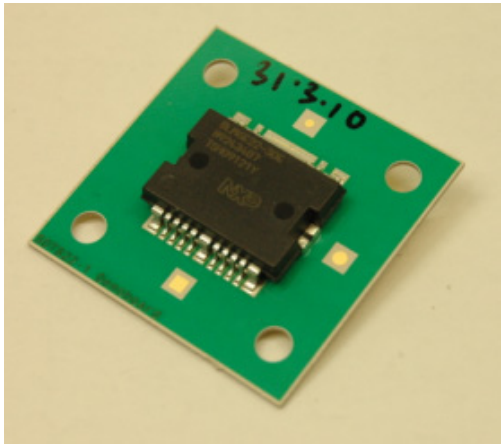


Fig 27. Example of surface mounted device

Common board finishes include NiAu, Organic Solder-ability Preservative (OSP), and immersion Sn. Although finishes may look different after reflow, and some appear to have better wetting characteristics than others, all common finishes can be used, provided that they are in accordance with the specifications. Examples of other issues in board quality are tolerances on the pad and solder resist dimensions and component placement, maximum board dimensions, and flatness. The application board is usually a mix of large and small components together with thermal design features. In board designs where large components or thermal design features are in close proximity to small components, solder-ability issues may arise.

4.2 Stencil aperture

A general rule is that the stencil apertures must be 25 um smaller than the solder lands, on all sides. In other words, the solder paste lays 25 um inward from the solder land edge. This usually results in stencil aperture dimensions that are 50 um smaller than the corresponding solder land dimensions; see Fig 28.

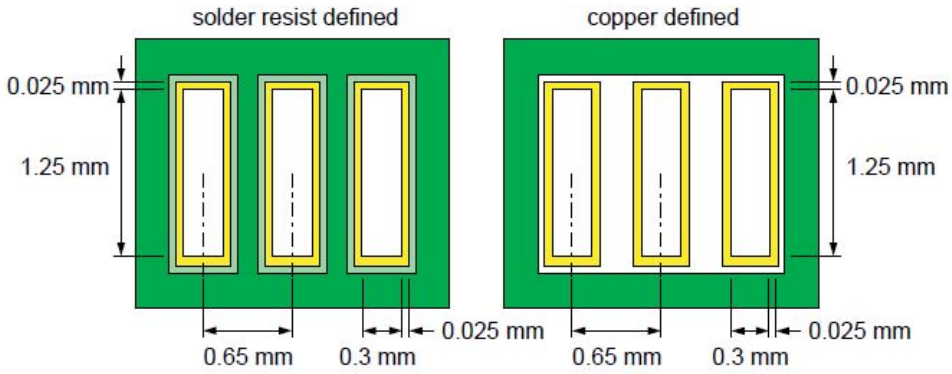


Fig 28. Solder paste printing on NSMDP and SMDP

Another exception lies with the very large solder lands, such as when printing solder paste on a heat sink land. In that case, it is advised to print an array of smaller solder paste deposits. The solder paste should cover approximately 20 % of the total land area. It is also advised to keep the solder paste away from the edges of this land: the solder paste pattern, including the spacing between the deposits, should have coverage of 35 % of the land area; see Fig 29. and Fig 30.

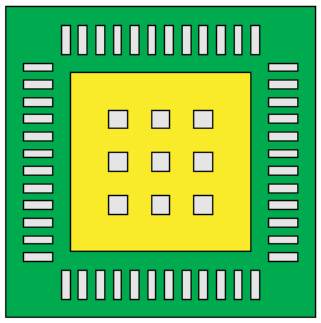


Fig 29. Solder paste printing on NSMDP and SMDP

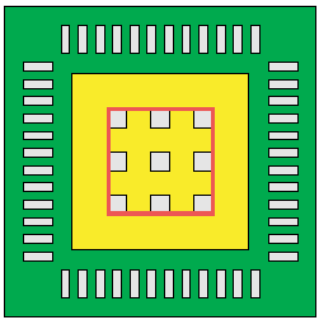


Fig 30. Solder paste printing on NSMDP and SMDP

A paste-printing pattern for exposed die pads is illustrated by the example shown in Figure 31. A HVQFN48 with an exposed pad of 5.1 mm x 5.1 mm, for example, should have nine solder paste deposits that are arranged in a three-by-three array. The solder paste deposits are 0.76 mm x 0.76 mm, and the distance between them is 0.37 mm.

This way, the solder paste area is 9 x (0.76 mm x 0.76 mm), and dividing this by the land area 5.1 mm x 5.1 mm yields a solder paste coverage of approximately 20 %. Similarly, the solder paste pattern (the paste, plus the area between the deposits) has a length of

3.02 mm. The pattern area, 3.02 mm x 3.02 mm, divided by the land area, yields a solder past pattern coverage of approximately 35 %.

Depending on the solder paste used, the solder paste deposits printed on a large land may not always coalesce completely. In some cases, individual solder joints can still be recognized between the exposed die pad and solder land on the board. It is possible that voids remain in the solder joints. Whether or not voids or incomplete coalescing of the solder are a problem, depends on the application. For low-power devices in which little heat is generated, up to 80 % of voids may still be acceptable.

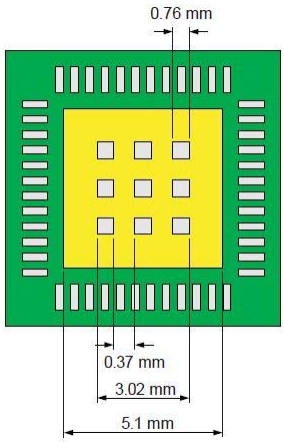


Fig 31. Solder paste dimensions on the land area for an exposed die pad

5. Solder past and preform

There are several materials that ensure a good thermal and electrical conductive interface. In Table 2 gives a summary of the possible combinations. The “X” marked cells are typically used in the industry while the ”O” marked cells might be optional.

Table 2. Overview of solder pastes and preforms used
(X = commonly used, O = optional)

Lead shape and solder type	Air cavity				Over molded			
	Eared		Earless		Eared		Earless	
	Leads	Flange	Leads	Flange	Leads	Flange	Leads	Flange
S = Straight, G = Gull wing	S	-	S	-	-	-	S & G	-
Solder paste	X	-	X	O	-	-	X	X
Solder preform	O	-	O	X	-	-	-	O
Thermal paste	-	X	-	-	-	-	-	-

5.1 Solders

In line with European legislation, it is recommended to use a Pb-free solder paste or preform, although exemptions are granted for selected applications, such as automotive.

A wide variety of Pb-free solder pastes are available, containing combinations of tin, copper, antimony, silver, bismuth, indium, and other elements. The different types of Pb-free solder pastes/preforms have a wide range of melting temperatures. Solders with a high melting point may be more suitable for the automotive industry, whereas solders with a low melting point can be used for soldering consumer semiconductor packages.

As a substitute for SnPb solder, the most common Pb-free paste/preforms is SAC, which is a combination of tin (Sn), silver (Ag), and copper (Cu). These three elements are usually in the range of 3 % to 4 % of Ag and 0 % to 1 % of Cu, which is near eutectic. SAC typically has a melting temperature of around 217 °C, and it requires a reflow temperature of more than 235 °C.

Table 3. Minimum peak temperature for soldering

Solder	Melting temperature	Minimum peak reflow temperature (measured at the solder joint)
SAC	217 °C	235 °C
PbSn	183 °C	215 °C

Care should be taken when selecting a solder, and note that solder types are categorized by solder sphere size. For small packages or fine pitch applications solder paste type 3 or better is recommended.

A no-clean solder paste or preform does not require cleaning after reflow soldering and is therefore preferred, provided that this is possible within the process window. If a no-clean paste is used, flux residues may be visible on the board after reflow.

Preforms with pre-applied flux are available in market.

In case separate flux (manually, like with a brush, pen or dipping) is applied in combination with a preform, extra care needs to be taken not too use excessive amounts of flux. These might increase the chance of voids in the solder joint.

For more information on the solder paste and solder preforms, please contact your solder supplier.

5.2 Thermal paste/preform

The eared (bolt down) ceramic packages are typically using a thermal paste or preform to improve the thermal conductivity, meaning better than a metal on metal contact. A “metal to metal” contact area is very small (could be ~ 2 % depending on the roughness). Applying pressure by bolt down will increase this contact area, but still those areas not being in contact are filled up by air, known as a bad heat conductor.

Filling these air pockets with a thermal paste (in lesser extend with a preform) will increase the contact area further resulting in a better thermal conductivity.

Solder offers the best thermal contact but can create other problems such as trapped flux (voids) and TCE mismatch (bow).

NXP does use thermal grease for the evaluation of eared (bolt down) and solder preforms for the earless devices.

For production reasons (efficiency) customers use thermal preforms, such as metal foils (like copper) and graphite containing pads.

Point of attention when pads are used:

- Check for galvanic corrosion in the application.
- Keep the pad size close to the size of the backside of the device. Too short pads give additional stress when bolting down the flange ands might even cause cracking of the package.

5.3 Solder amount

This document does not give recommendation about the amount of solder to be used for every type of product. For air cavity packages however it is important to take notice of the gold plating. In 10.3 the information needed to prevent gold embrittlement can be found.

6. Reflow soldering procedure

NXP advises to use a convection oven rather than a conduction or radiation oven. A convection oven provides a uniform heat and a very controlled temperature (± 2°C). Moreover, it allows soldering a wide range of products due to the temperature uniformity. During the reflow soldering process all parts of the board are subjected to an accurate temperature/time profile.

A temperature profile essentially consists of three phases:

- **Pre-heat:** the board is warmed up to a temperature that lies lower than the melting point of the solder alloy.
- **Reflow**: the board is heated to a peak temperature well above the melting point of the solder, but below the temperature at which the components and boards are damaged.
- **Cooling down:** the board is cooled down, so that soldered joints freeze before the board exits the oven.

The peak temperature during reflow has an upper and a lower limit.

6.1 Lower limit of peak temperature

The minimum peak temperature must at least be high enough for the solder to make reliable solder joints. This is determined by solder paste characteristics; contact your paste supplier for details.

6.2 Upper limit of peak temperature

The maximum peak temperature must be lower than the temperature at which the components are damaged. This is defined by MSL testing of the package. The maximum body temperature during reflow soldering depends on the body size and on the demand to respect the package MSL.

6.3 The temperature at which the boards are damaged

This is a board characteristic; contact your board supplier for details.

When a board is exposed to the temperature profile, certain areas on the board will become hotter than others: a board has hot spots (the hottest areas) and cold spots (the coolest areas). Cold spots are usually found in sections of the board that hold a high density of large components, as these soak up a lot of heat, or near heat sinks. Hot spots, on the other hand, are found in areas with few components, or only the smallest components, and with little Cu nearby. Finally, the board dimensions, and the board orientation in the oven, may also affect the location of hot and cold spots.

The hot spot on a board may not surpass the upper limit to the peak temperature. Similarly, the cold spot must reach the lower limit at least. Thus, it is imperative that all areas on the board, including the hot and cold spots, fall within the upper and lower limits of the peak temperature.

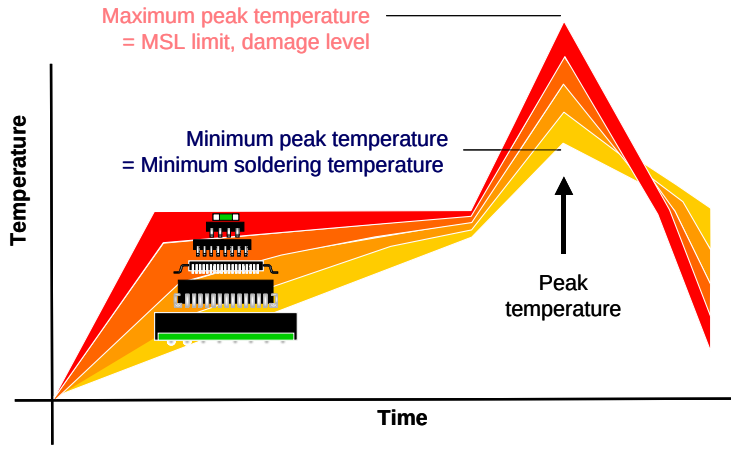


Fig 32. Temperature profiles for large and small components

In Fig 32 the yellow band with the large component represents cold spots, and the red band, with the smallest component, represents hot spots. In the pre-heat phase, the hot spots will heat up rapidly to a temperature lower than the melting point of the solder alloy. They may remain at this temperature for a while. Note, however, that small solder paste deposits should not remain at an intermediate temperature for so long that their activator runs out: for small solder paste deposits, a fast temperature profile is preferred. The cold spots on the board will warm up far more slowly. The oven settings should be planned so that the cold as well as the hot spots will have reached roughly the same temperature by the end of the pre-heat phase.

The second phase in the reflow profile is the reflow zone, in which the solder melts and forms soldered joints. The minimum peak temperature, in which all solder joints in the cold as well as the hot spots must reach, depends on the solder alloy. However, no region on the board may surpass a maximum peak temperature, as this would result in component and/or board damage. Even if the cold and hot spots start the reflow phase with roughly the same temperature, the hot spots will reach a higher peak temperature than the cold spots. Yet, both the hot spots and the cold spots must lie within the allowed peak temperature range. This may require some tweaking of the oven temperature settings and conveyor belt speeds. In extreme cases, even the board layout may have to be optimised to limit the temperature difference between the cold and the hot spots.

When reflow soldering, the peak temperature should never exceed the temperature at which either the components or the board are damaged. The maximum peak temperature for components is partially determined by their moisture sensitivity. For reflow soldering with SnPb solder, the peak temperature should be larger than 210 ºC; when soldering with SAC, the peak temperature should be larger than 235 ºC. Note that this usually implies a smaller process window for Pb-free soldering, thus requiring tighter process control.

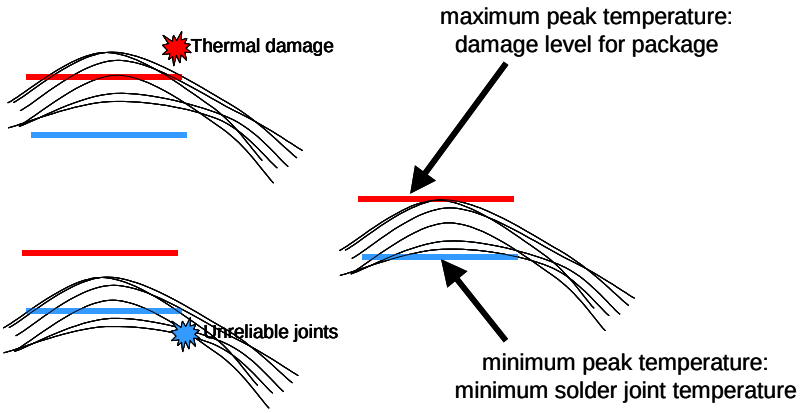


Fig 33. Fitting both the hot and cold spots into the required peak temperature range

The black lines in Fig 33 represent the actual temperature profiles for a number of different spots on a board. The bottom line represents the cold spot, and the top line corresponds to the hot spot. The blue line represents the minimum allowed peak temperature, and the red line is the maximum allowed peak temperature. At the top left, some regions on the board are exposed to temperatures that are too high, resulting in damage. At the bottom left, some regions on the board are exposed to temperatures that are too low, resulting in unreliable joints. At the right, all of the regions on the board have peak temperatures that fall within the upper and lower limits.

Reflow may be done either in air or in Nitrogen. In general, nitrogen should not be necessary; in that case, air is preferred because of the lower cost. Reflow may be done in convection reflow ovens, some of which have additional infrared heating. Furthermore, using vapour phase reflow soldering can reduce temperature differences on a board.

Proper joint formation should always be verified by visual inspection through a microscope. In general, Pb-free solder is a little less successful at wetting than SnPb solders; SAC fillets will have a larger contact angle between the fillet and the wetted surface. When using Pb-free solder this contact angle may typically be 20° to 30°. In paragraph 7 more information is given concerning wetting behaviour.

6.4 An example of a reflow profile used for internal study:

Calibration:

The reflow soldering profile should be calibrated with a thermo couple glued down on the cap of the ACP device to prevent a temperature offset.

All reflow activities were performed in the Heller oven (Model 1700 EXL) with 6 zones, and reflow was in an inert atmosphere (N_2). An inert atmosphere improves wetting and reduces the chances of solder balling. This is a belt oven, and changing zone temperatures and belt speed can alter temperature profiles. The monitored temperature profiles are compared to the JEDEC recommendations (Table 4).

Table 4. Reflow profile classification (JEDEC JSTD020d)

Parameter	Units	Specification	Comments
Time above liquidus	s	60 – 150	SAC Liquiqus is 217 °C
Ramp-up slope (max)	°C / s	3	Heating rate
Max. package temperature	°C	245	

The solder used was SAC (Pb-free) with a melting point of 217 °C, and peak-soldering temperature was between 235 °C to 245 °C (JEDEC JSTD020d). The reflow profile shown in Table 5 provided the measured output parameters presented in Table 6.

Table 5. Reflow oven settings – zone temperature and belt speed

Zone #	1	2	3	4	5	6	Belt speed
Temperature (°C)	150	155	170	230	245	260`	36 cm/min

Table 6. Measured temperature profile

Parameter	Units	Spec	Measured value
Time above liquidus	s	60 – 150	83
Ramp-up slope (max)	°C / s	3	1.71
Max package temperature	°C	245	239

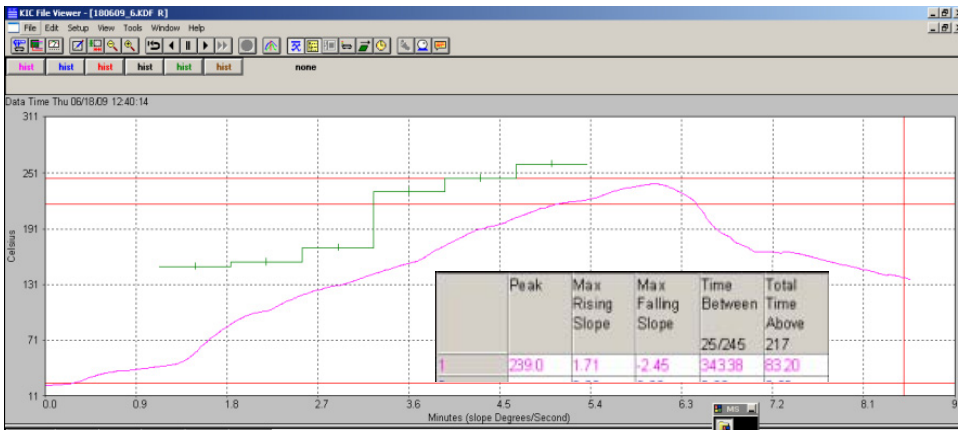
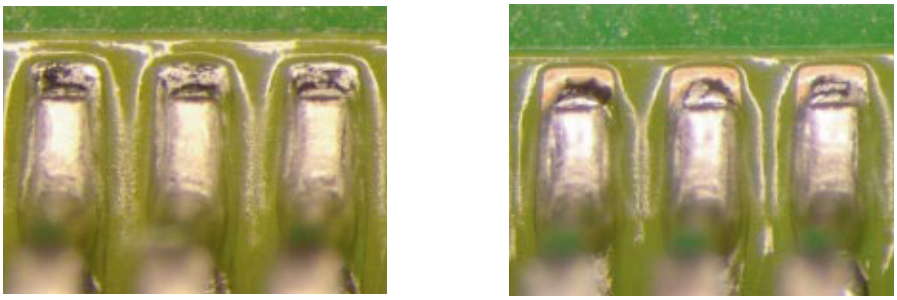


Fig 34. Measured reflow profile

7. Inspection

7.1 Wetting appearance

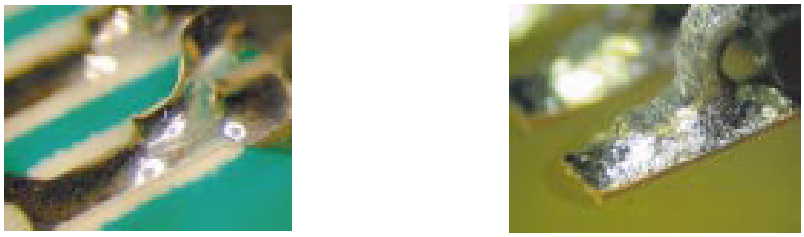
Notice the difference between SnPb and Pb-free solder in Fig 35 the photograph on the left (SnPb) shows the solder lands have been wetted completely. The photograph on the right shows the solder has left part of the solder lands non-wetted.



a. SnPb solder joints

b. Pb free solder joints

Fig 35. Wetting appearance



c. SnPb solder joints

d. Pb free solder joints

Fig 36. Visual appearance (shiny versus dull)

Another visual aspect in Pb-free soldering is that Pb-free solder joints tend to be less shiny than SnPb solder joints and they may have striation marks. This is due to the different microstructure that is formed during solidification. Although SnPb solder joints should be rejected if they look this way, this is normal for Pb-free and no reason to reject Pb-free solder joints.

Non-wetting of lead frame parts as a result of punching or sawing is not a reason for rejection. Other inspection methods besides optical inspection, such as, for design and process development purposes are:

- Automatic optical inspection (AOI)
- Examination by roentgen ray (X-ray)
- Cross-sectional analysis
- Dye penetration test
- CSAM (scanning acoustic microscope)

7.2 X-ray

X-ray can only provide information between the leads and laminate interface. Void levels under 10 % do provide confidence in the materials and soldering process.

In the Fig 37 an example can be seen of voiding under the lead tip.

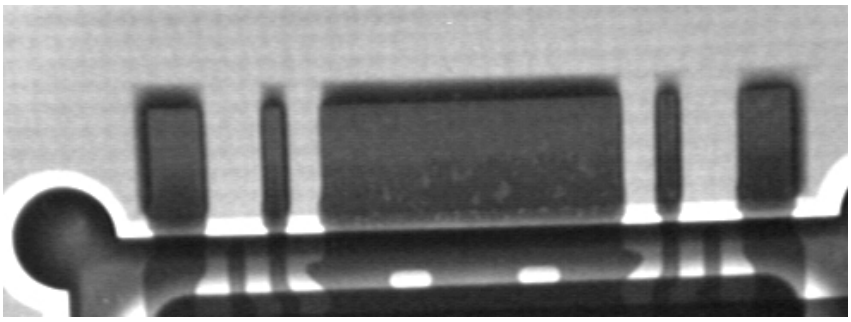


Fig 37. X-ray lead-PCB interface

7.3 C-SAM

This method is used to examine in particular the interface between the exposed heat spreader/flange and the heat sink, as it is not detectable by x-ray. Variability in gray scale (dark – bright) indicates presence of voids.

In several demo boards, the solder interfaces are in the same plane. Consequently focusing is required only on one plane. The interface between the heat spreader and heat sink shows very little variation, which implies low level of voids.

8. Mounting procedure

8.1 Air cavity devices

8.1.1 Manual mounting

8.1.1.1 Package placement

Even though the ceramic package is not passed through a reflow oven, it may be heated by a soldering iron or bar. Therefore, for the sake of moisture sensitivity, it is best to store the packages in dry environment or in Nitrogen.

Using an in-house method, apply an even layer of thermal compound to the bottom of the package flange. This thermal compound will improve the thermal conductivity between the metal surfaces of the flange and the heat sink. The layer must be thin, and it must be evenly spread out before placing the package, so that no air bubbles are trapped. Use of excessive thermal compound is not desirable, as it adds a “layer” of thermal resistance. In addition, excess thermal compound may leak out of the heat sink cavity when the package is bolted to the heat sink – this could contaminate the PCB near the package.

Place the package in its position, with the flange sticking through the PCB and into the cavity in the heat sink. Package alignment is done visually, by adjusting the position so that the package leads are exactly aligned with the PCB pads.

In order to ensure a good interconnection between the flange and the bottom of the heat sink cavity, the package is bolted down onto the heat sink. The holes in the heat sink may have thread, in which case the bolt is fixed to the heat sink itself. They may also be plain, in which case nuts are used to tighten the bolts. Both situations are illustrated in Fig 38.

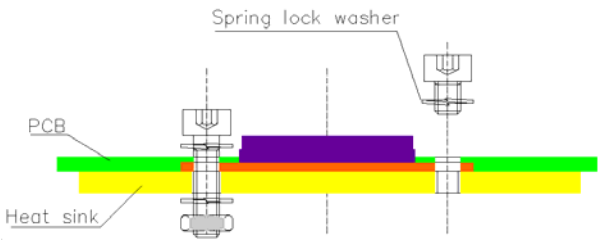


Fig 38. Main rules in defining the SMD footprint

Do not use hexagonal bolts, as these may interfere with some of the smaller flange-mount packages during the bolting step.

The force applied when tightening the bolts is important to ensure a good contact between the flange and the heat sink. It is recommended to tighten the bolts in two steps to ensure the packages free from damages during mounting:

- First, both bolts should be tightened (finger tight).
- Second, the bolts should be fully tightened to the recommended torque with a controlled torque wrench, such as a torque screwdriver. Excessive torque may damage the device. The range of torques (calculated for M3) recommended for flange packages.

Table 7. Torque

Torque	Minimum value	Maximum value
Nm	0.60	0.75

Washers are recommended in order to spread the force equally. In addition, use of spring-lock washers will make sure that the bolts do not come loose with vibrations when the product is used.

8.1.1.2 Soldering the leads

Soldering the leads to the PCB pads is largely a question of good workmanship, as it is done manually. Use a soldering iron, or bar, with a tip that is at least as wide as the leads. The width should be smaller than the package width, to eliminate the risk of accidentally touching other components on the PCB.

Use a soldering iron or bar that is ESD-safe.

Use solder wire. Use an alloy that has a melting temperature that is not higher (and preferably lower) than the solder that was used on the rest of the PCB. Set the soldering iron or bar to the temperature specified by the solder supplier. Flux containing solder wire is preferred.

Using the iron or bar, apply solder to the PCB pad, around the package lead. Make sure that the solder has melted completely and apply enough solder to ensure a good joint. If there is a small gap between the lead and the pad apply extra solder to fill this. Throughout this process care must be taken that the soldering iron or bar makes contact with neither the package body nor the neighboring components. The solder may not touch the package body.

Proper joint formation should be verified by visual inspection through a microscope. If there is a gap between the leads and the PCB pad, check the filling by the solder. Also, an angle of 20° – 30° degrees indicates good wetting, for lead-free solders.

8.1.1.3 Reflow mounting

For these packages, it is critical the leads make good contact with the pads on the PCB, and that – at the same time – the flange makes good contact with the heat sink. For these reasons, the package is usually bolted to the board with a fixture, during reflow.

Firstly, the package must be placed on the PCB and into the heat sink cavity, in such a way that the flange makes contact with the bottom of the heat sink cavity. At the same time, contact between the leads and the PCB pads may not be optimal. Next, the fixture is bolted down over the package, so that good contact between the leads and the PCB pads are also ensured. This is described in more detail in the following sections.

8.1.1.4 Fixture Design

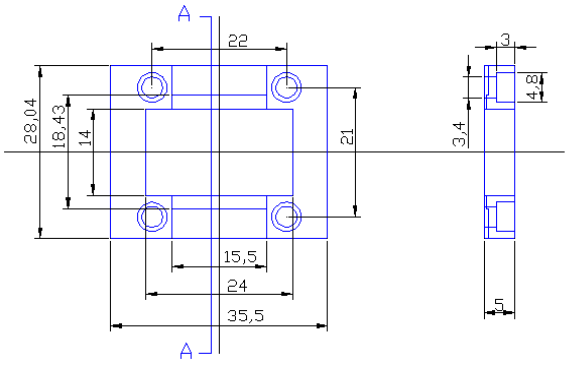


Fig 39. Fixture dimensions

These ceramic packages should be fixed to the PCB using a fixture. The fixture is bolted to the heat sink, with bolts that pass through the PCB. In Fig 39.an example of a fixture can be seen.

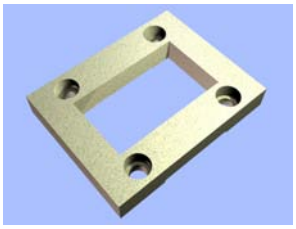


Fig 40. Fixture top view

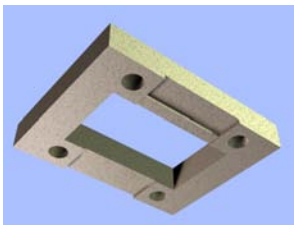


Fig 41. Fixture bottom view

The fixture has a small ridge that presses down on the package leads. A close-up of this ridge is shown in Fig 42.

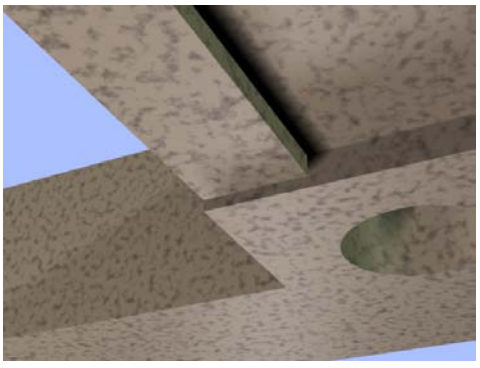


Fig 42. Close-up of ridge in fixture

The package is placed in the heat sink cavity through an aperture in the PCB.

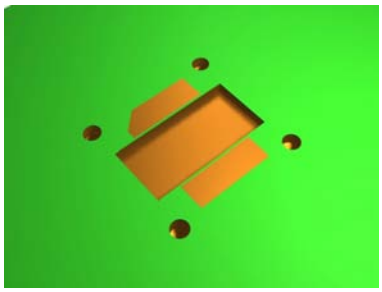


Fig 43. Example apertures in the PCB

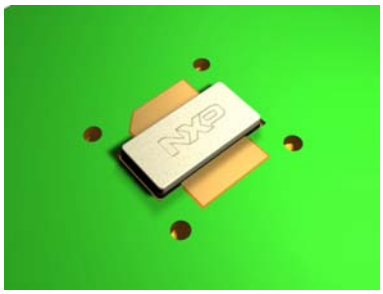


Fig 44. Placed device

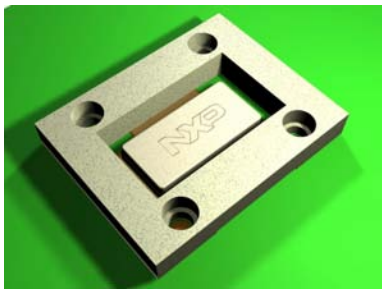


Fig 45. Placed fixture

The fixture is also bolted through holes in the PCB.

Place the package in its position, with the flange sticking through the PCB and into the cavity in the heat sink. Package alignment is done visually, by adjusting the position so that the package leads are exactly over the PCB pads. If the depth of the heat sink cavity was designed correctly, contact should be made between the package leads and the printed solder paste. The package leads should ideally be pressed at least 20 µm into the solder paste. In some cases, however, depending on the various values in the stack in the z direction, and on tolerances, the leads may also hover above the solder paste.

Verify manually that the package flange rests on the solder preform that has been placed in the heat sink cavity. If the cavity is too deep, so that the package flange does not make good thermal contact with the bottom of the heat sink cavity, a thicker preform may be used – but keep the R_{th} increase in mind.

It must be stressed that it is acceptable at this point in the process if the leads do not make contact with the solder paste, but it is not acceptable if the flange does not make contact with the solder preform. In order to ensure a good interconnection between the leads and the pads on the PCB, a reflow fixture is now bolted down over the package, onto the heat sink. The bolts pass through holes in the PCB. The holes in the heat sink may have thread, in which case the bolt is fixed to the heat sink itself. The bolts may also be plain, in which case nuts are used to tighten the bolts.

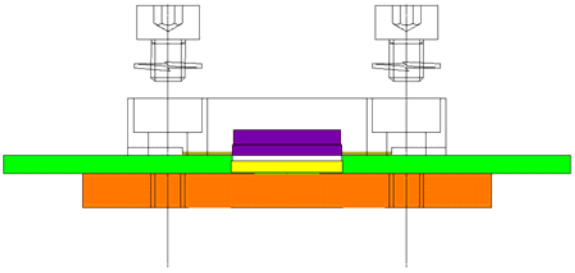


Fig 46. Bolting down the reflow fixture

It is recommended that the bolts be tightened in two steps:

- First, the bolts should be tightened by hand so they are finger tight.
- Second, the bolts should be fully tightened to the recommended torque with a controlled torque wrench, such as a torque screwdriver.

A difference in torque between bolts may lead to a tilted reflow fixture and joints that have not been soldered properly.

Table 8. Suggested torque ranges for bolting down the fixture

Torque	Minimum value	Maximum value
Nm	0.60	0.75

The maximum recommended torques were calculated for M3 bolts.

After bolting down the fixture, check to make sure that the package leads make good contact with the solder paste

The tips of the leads should be pressed at least 20 µm into the solder paste. If there is no proper contact between the leads and the solder paste, extra solder paste can be dispensed onto the leads.

The leads may not be bent downward more than 300 µm. After bolting down the fixture, make sure that this is not the case. The reason for this limit is that too much lead deflection may cause great mechanical stress at the lead/body interface, causing damage to the package.

8.1.1.5 Reflow soldering

The most important step in reflow soldering is when the solder paste deposits melt and soldered joints are formed. This is achieved by passing the boards through an oven and exposing them to a temperature profile with varied times.

A rough indication of the recommended minimum peak temperatures for SnPb and SAC alloys is given in Table 3, however, these values should be verified with your solder paste supplier.

After reflow, check that the solder in the heat sink cavity does not make contact with the package body.

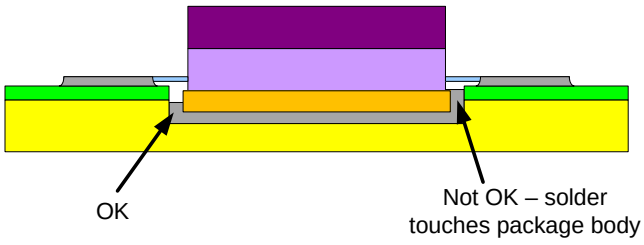


Fig 47. Inspection of solder

Finally, remove the reusable reflow fixture.

8.2 Over molded devices

8.2.1 Manual mounting

8.2.1.1 Package placement

The required placement accuracy of a package depends on a variety of factors, such as package size and the terminal pitch, but also the package type itself. During reflow, when the solder is molten, a package that has not been placed perfectly may center itself on the pads: this is referred to as self-alignment. Therefore, the required placement accuracy of a package may be less tight if this package is a trusted self-aligner. It is known, for example, that a BGA is good at self-alignment, as the package body essentially rests on a number of droplets of molten solder, resulting in minimal friction.

Remark: Self-alignment properties can be improved by performing the reflow process in an N2 environment.

Typical placement tolerances, as a function of the semiconductor package terminal pitch, are given in Table 9.

Table 9. Typical placement accuracy

Package terminal pitch	Placement tolerance (3 sigma)
> 0.65 mm	100 μm
< 0.65 mm > 0.5 mm	50 μm
< 0.5 mm	30 μm

Semiconductor packages are usually placed with two types of machines. If the highest placement accuracy is required, the slower but more accurate machines must be used. These machines are also often more flexible when it comes to unusual package shapes, that may require dedicated nozzles and non-standard trays. If the highest placement accuracy is not necessary, and there are no special requirements, fast component mounters or chip shooters, can be used. These machines can process up to 100,000 components per hour.

The placement force may also be an important parameter for some packages. In theory, a semiconductor package is always pressed down into the solder paste until it rests on a single layer of solder paste powder particles - the rest of the solder paste is pressed aside. A consequence immediately apparent is that the solder paste that is pushed aside, or that bulges outside the package, may cause bridges with neighboring solder paste deposits.

In extreme cases, solder paste may not only bulge outside the pads, but may actually be blasted further away from the pads, so that a small amount of solder paste is no longer connected to the paste deposit it originally came from. This must always be avoided as the splattered solder paste may cause a short circuit on the board, and the original solder paste deposit may then have insufficient solder. Incidentally, this effect is often caused in part by use of an improper nozzle shape, so that the paste is actually blown away by air from the nozzle.

If the placement force is too low, there is a chance that a semiconductor package terminal does not make sufficient contact with the solder paste. In that case, there is a risk that the solder paste tackiness will not be able to hold it in place up to the reflow zone in the oven, and the package may be displaced. In addition, even if the semiconductor package remains in place, there may be bad contact between the package terminals and the solder paste resulting in open contacts or bad joints.

Therefore, the placement force must always be adjusted so that there is no excessive paste bulging or even splattering and there is a proper contact between the semiconductor package and the solder paste. The necessary placement force to achieve this will depend on a number of factors, including the package dimensions. Typical forces are 1.5 N to 4 N. Note however, that some of the more modern machines have a sensor that detects the package's proximity to the solder paste so that the placement speed is reduced as soon as the package comes near to, or touches, the solder paste. In this way, splattering can be minimized.

9. Reworking

A package lead, not being soldered properly, can be repaired by heating it with the tip of a soldering iron. In that case, it is sufficient to heat the lead until the solder melts completely, and a new device should not be necessary.

In other situations, however, there may be a need to replace the package. In that case, the rework process should consist of the following steps:

- Removal of old package
- Site preparation
- New package placement
- Soldering new package

9.1 Removal of the package

Prior to removal of the old package it is advised to dry-bake the PCB for 4 hours at 125 ^{o}C, then:

- Unscrew the bolts holding down the eared package.
- Remove the old package using a specially designed soldering iron tip. The tip may have two parts pressing down on the two leads at the same time, and leave room in the middle for a nozzle to lift the component. Examples of special tips for soldering irons are shown in Fig 48.

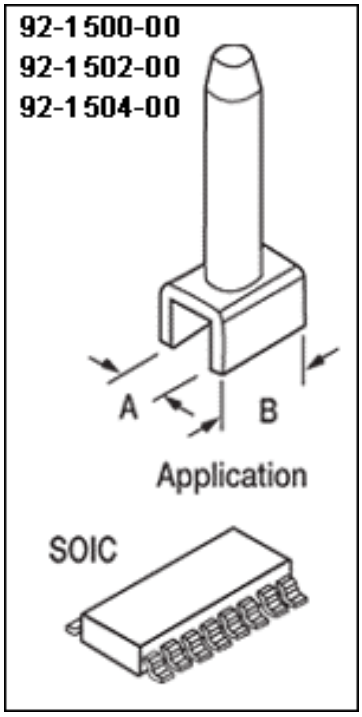


Fig 48. Two part soldering iron tips

If the package is going to be submitted to a failure analysis, use a soldering iron that is ESD-safe.

It is essential that both leads are heated simultaneously, while a vacuum wand nozzle is attached to the top of the package body, for lifting it off.

The process steps are as follows:

- Set the soldering iron or bar to a temperature that is high enough to melt the solder. This value depends on the solder that was used to attach the package.
- Attach a vacuum wand nozzle to the top of the package body.
- When the soldering iron has reached the desired temperature, place it over the package so that both package leads are heated simultaneously.
- Watch carefully as the soldering iron or bar heats the solder joint.
- As soon as the solder melts, lift the package off the PCB using the vacuum wand. Do not lift the package before the solder in the joints has melted completely, as this may damage the package and the PCB.

Throughout this process, care must be taken that the soldering iron or bar makes contact with neither the package body nor the neighboring components.

Although a hot air gun with a dedicated nozzle could theoretically be used, this is not recommended. With hot air guns, the package body is also heated, and the temperatures are often poorly defined.

If a soldering iron with a suitable tip is not available, it is possible to remove the old package by de-soldering the leads one lead at a time. In that case, apply the iron to one of the leads, and wait until the solder in the joint has melted completely. Then, lift the package. As the other lead is still soldered to the PCB, this will result in damage. Next, de-solder the other lead. Due to the damage this method causes, it is not preferred if the package is going to be submitted for failure analysis.

After the old package has been removed, check whether excess thermal compound has remained in the cavity in the heat sink. If this is the case, remove the heat sink from the PCB and discard it.

9.2 Site preparation

After the package has been removed, the PCB pads must be prepared for the new package. Prepare the pads by removing any excess solder and/or flux remains. Ideally this is done on an appropriate de-soldering station. Alternately, use a soldering iron set to the temperature specified for the solder that was originally used to attach the package. Clean the pads using the soldering iron and solder wick, or another in-house technique. Note: use a temperature that is needed to just liquefy the solder but that does not damage the PCB.

After most of the solder has been removed from a solder land, a very thin layer of solder will be left, on top of a few intermetallic layers. In the case of Cu pads, for example, there will be layers of Cu_3Sn, Cu_6Sn_5, and finally solder, on top of the Cu. The top layer of solder is easily solder-able.

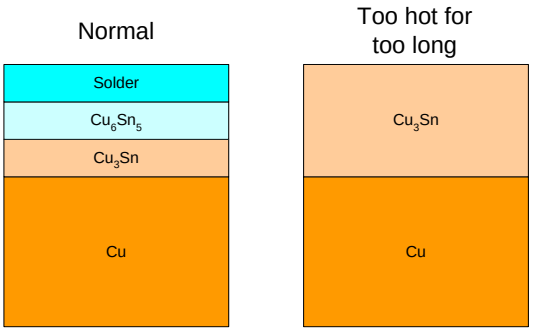


Fig 49. Overheating and Cu_3Sn formation

If, however, the pad is heated too much during removal of the rejected IC package, and during site preparation, the top two layers will also be converted into Cu_3Sn; in that case, there will only be the Cu_3Sn inter-metallic layer on top of the Cu. Unfortunately, Cu_3Sn is hardly wettable. As a result, it will become very difficult to solder the replacement package at this location. Therefore, care must be taken during reject package removal and site redress, that the solder lands are heated only as much as is absolutely necessary.

9.3 Placement of the new package

If the heat sink was discarded, mount a new heat sink. Next, mount a new package in much the same way as the original package was mounted. Re-use of removed packages is not recommended. Finally, the new package is soldered to the PCB in the same manner as the original package.

10. Appendices

10.1 Appendix I: MSL

If there is moisture trapped inside a plastic over molded surface mount package, and the package is exposed to a reflow temperature profile, the moisture may turn into steam, which expands rapidly. This may cause damage to the inside of the package (delamination), and it may result in a cracked semiconductor package body (the popcorn effect). A package's sensitivity to moisture, or Moisture Sensitivity Level (MSL), depends on the package characteristics and on the temperature it is exposed to during reflow soldering. The MSL of semiconductor packages can be determined through standardized tests in which the packages are moisturized to a predetermined level and then exposed to a temperature profile. Studies have shown that small and thin packages reach higher temperatures during reflow than larger packages. Therefore, small and thin packages must be classified at higher reflow temperatures. The temperatures that packages are exposed to are always measured at the top of the package body. Depending on the damage after this test, an MSL of 1 (not sensitive to moisture) to 6 (very sensitive to moisture) is attached to the semiconductor package. For every plastic over molded product, this MSL is given on a packing label on the shipping box. Each package is rated at two temperatures, for SnPb and Pb-free soldering conditions. An example of a packing label is given in Fig 50.

Fig 50. Example of MSL information on packing label; note the two MSLs corresponding to the two reflow processes

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow, in order to remove any moisture that might have soaked into the package. MSLs and temperatures on the packing labels are to be respected at all times. Naturally, this also means that semiconductor packages with a critical MSL may not remain on the placement machine between assembly runs. Nor should partial assembled boards, between two reflow steps, be stored longer than indicated by the MSL level. The semiconductor package floor life, as a function of the MSL, can be found in Table 10.

Table 10. MSL levels

MSL	Floor life	
	Time	Conditions
1	Unlimited	≤ 30 °C / 85 % RH
2	1 year	≤ 30 °C / 85 % RH
3a	4 weeks	≤ 30 °C / 85 % RH
3	168 hours	≤ 30 °C / 85 % RH
4	72 hours	≤ 30 °C / 85 % RH
5	48 hours	≤ 30 °C / 85 % RH
5a	24 hours	≤ 30 °C / 85 % RH
6	6 hours	≤ 30 °C / 85 % RH

Note: The definition of surface mount implies to have the exposed heat spreader and the lead surface to be at the same level. With other words an over molded package with straight leads is not purely surface mount.

The MSL levels are normally determined for only surface mount devices (typically gull wing), but NXP also specifies the MSL level for Plastic over molded packages containing straight leads.

10.2 ESD

Damage to semiconductors from Electro Static Discharge (ESD) is a major cause of rejects and poses an increased risk to miniaturized packages. Electrostatic charge can be stored in many things, for example, man-made fiber clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. It is recommended that the following ESD precautions be complied with.

10.2.1 Workstations for handling ESD sensitive components

Fig 50 shows a working area suitable for safely handling electrostatic-sensitive devices. The following precautions should be observed:

- Workbench and floor surface should be lined with anti-static material
- Persons at a workbench should be earthed via a wrist strap and a resistor
- All mains-powered equipment should be connected to the mains via an earth leakage switch
- Equipment cases should be grounded
- Relative humidity should be maintained between 40 % and 50 %
- An ionizer should be used to neutralize objects with immobile static charges in case other solutions fail
- Keep static materials, such as plastic envelopes and plastic trays away from the workbench. If there are any such static materials on the workbench remove them before handling the semiconductor devices.
- Refer to the current version of the handbook EN 100015 (CECC 00015) “Protection of Electrostatic Sensitive Devices” (see 12), which explains in more detail how to arrange an ESD protective area for handling ESD sensitive devices.

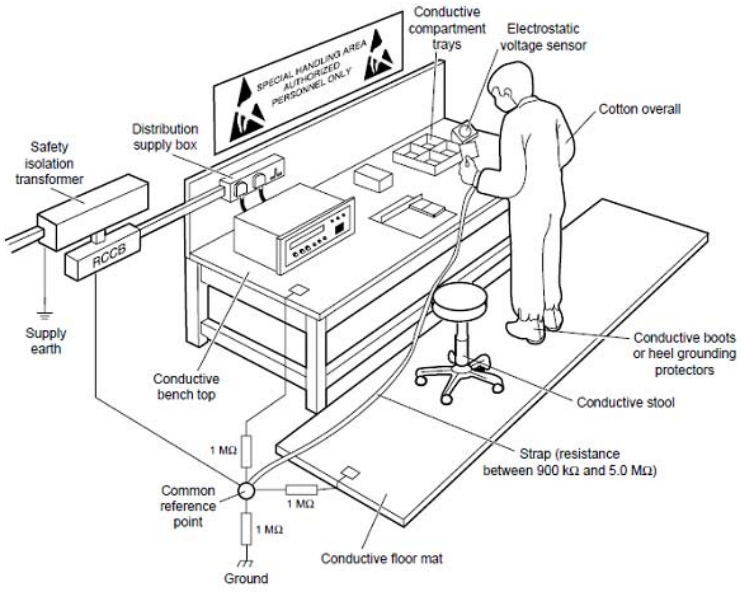


Fig 51. Work place

10.2.2 Receipt and storage of components

Packing for electrostatic devices should be made of anti-static/conductive materials.

Warning labels on both primary and secondary packing show that the contents are sensitive to electrostatic discharge. The electronic components should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be done at a protected workstation. Any electronic components that are stored temporarily should be re-packed in conductive or anti-static packing or carriers.

10.2.3 PCB assembly

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand tools should be of conductive or anti-static material and where possible should not be insulated. Standard precautions for manual handling of electrostatic-sensitive devices need to be taken into account.

10.3 Gold embrittlement

Air cavity packages are gold plated. In order to avoid brittle AuSn inter-metallics (reliability) in the solder joints enough solder should be applied. The level of gold within the solder joint may not exceed 4% by weight.

10.3.1 Solder paste

NXP used Pb-free solder 95.5Sn3.8Ag0.7%Cu SAC for its evaluation. This solder paste contained 88% w/w[1] of powdered solder alloy (96SC) and 12% w/w flux. The density of the Sn3.8Ag0.7Cu Pb-free solder alloy is approximately 7.5 g/cc.

10.3.2 Flange to Heat sink attachment

Required amount of solder (after the reflow soldering step):

$\mathbf{W}eight_{Au} \leq 4\%\ \mathbf{W}eight_{total}$

$\mathbf{W}eight_{total} = \mathbf{W}eight_{Au} + \mathbf{W}eight_{solder}$

Therefore, the amount of solder required after reflow is calculated using,

$\mathbf{W}eight_{Au} = (\mathbf{V}olume_{Au}) \times \boldsymbol{\rho}_{Au} = (\mathbf{T}hickness_{Au} \times \mathbf{W}idth_{Flange} \times \mathbf{L}ength_{Flange}) \times \boldsymbol{\rho}_{Au}$

$\mathbf{W}eight_{Au} = (\mathbf{T}hickness_{Au} \times \mathbf{1} \times \mathbf{1}) \times \boldsymbol{\rho}_{Au}$ (for 1 unit of surface area)

$Weight_{Au} = (\mathbf{T}hickness_{Au}) \times \boldsymbol{\rho}_{Au}$

$\mathbf{W}eight_{total} = (\mathbf{T}hickness_{Au}) \times \boldsymbol{\rho}_{Au} + (\mathbf{T}hickness_{solder}) \times \boldsymbol{\rho}_{solder}$

(for 1 unit of surface area)

With:

- ρ is the density of the material. The density of gold is 19.3 g/cc
- $\mathbf{T}hickness_{Au}$ = 2.54 µm
- The density of solder is 7.5 g/cc
- $\mathbf{T}hickness_{solder}$ = **X** µm

To avoid brittle solder joint due to too much gold in the joint, **X** ≈ 150 µm solder thickness (only based on NXP part) is required for flange /heat sink attachment.

1. w/w : In relation to the weight and not to the volume

The difference in thickness before soldering and after reflow is about 50 %. Therefore, the thickness of solder paste to spread onto the soldering surface is Min 300 µm to ensure the Min 150 µm of solder required after reflow. Therefore, the thickness of stencil that should be used to spread the solder paste must be between 12 - 15 mils so that after re-flowing the solder layer thickness is more than 150 µm. It is tricky to ensure a proper and reliable soldering step with this amount of solder paste. It is also the reason why NXP advises to use Preform for flange to heat sink attachment.

10.3.3 Usage of a preform

NXP advises using preform with pre-applied flux for flange to heat sink attachment. It reduces voids and ensures the required amount of solder.

NXP recommend to use a Min 150 µm solder perform in order to ensure the required amount of solder (to avoid AuSn embrittlement of solder joints). The solder preform may not be less than 150 µm thick: note that a greater thickness will increase the R_{th} value.

10.3.4 Lead to PCB attachment

The leads are plated with a thinner Au layer compared to the flange: [0.8 µm – 1.27 µm]. Therefore, the thickness of solder required after soldering is about 75 µm.

As seen previously, the difference in thickness before soldering and after the reflow step is about 50 %. Therefore, the thickness of solder to spread onto the soldering surface (PCB pad) is about 150 µm. It allows ensuring about 75 µm of solder after the reflow step. A 6 mils stencil should then be used to evenly spread the solder paste.

11. Abbreviations

Table 11. Abbreviations

Acronym	Description
SnPb (solder)	Sn (Tin) Pb (Lead)
SAC (solder)	Sn (Tin) Ag (Silver) Cu (Copper)
MSL	Moisture Sensitivity Level
OMP (packages)	Over-Molded Plastic
RH	Relative Humidity
NSMDP	Non Solder Mask Defined Pads
SMDP	Solder Mask Defined Pads
PCB	Printed Circuit Board

12. References

[1] IPC/JEDEC J-STD-020D August 2007

Joint Industry Standard Moisture/Reflow, Sensitivity Classification for Non hermetic Solid State Surface Mount Devices

[2] IPC-7351

Generic requirements for Surface Mount Design and Land Pattern Standard, IPC

[3] EN 100015/CECC 00015

Protection of Electrostatic Sensitive Devices, European Standard

[4] 3997.750.04888

Quality reference handbook, NXP

[5] IPC-A-610D

Acceptability of Electronic Assemblies, IPC

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Date of release: 17 May 2010
Document identifier: AN10896_1